REMARKS

Claims 1-30 remain in this application. Claims 1, 15, 24 and 25 have been amended to put them into better form.

REJECTIONS TO THE CLAIMS UNDER 35 U.S.C. §§ 102(a) and 103(a)

Claims 1-13 and 15-30 were rejected as being anticipated under 35 U.S.C. § 102(a) U.S. Patent No. 5,713,030 to Evoy ("Evoy"). Claim 14 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Evoy.

Embodiments of the present invention pertain to reducing power consumption in a computer system by periodically reducing the power consumption of a processor. According to one embodiment shown in Fig. 1, a power reduction circuit includes a multiplexor 14 that receives a "select" input (line 20) from a failure signal generator which generates a signal based on a perceived failure condition (e.g., an inoperable fan, an excessive perceived temperature for the processor, etc.). Multiplexor 14 selects between two inputs, a power reduction inactive input (line 22) and signal generator 16 (line 24). In operation, if there is no failure condition (e.g., no signal generated by failure signal generator 12), then power reduction inactive signal (line 22) is passed to the output of multiplexor 14. If there is a failure condition, then a periodic signal from signal generator 16 is passed through to the processor 10. Accordingly, when a failure condition is present, multiplexor 14 sends the periodic signal to processor 10 to periodically reduce the power consumption of the processor. For example, the output signal (line 18) of multiplexor 14 can be coupled to the STPCLK input of processor 10 (e.g., a Pentium® processor). Thus, the periodic signal from signal generator 16 performs two operations with its periodically repeating high and

low signals: 1. Lets processor 10 operate at normal speed and 2. reduces power consumption of processor 10.

Evoy refers to a thermal management device for a computer processor. As shown in Fig. 3, the system of Evoy includes a processor chip 102 and a clock chip 104. Heat generated by the processor chip is detected by thermistor circuit 116, which generates a voltage for comparator 118. When the temperature is too high, the comparator generates a signal for the clock generator 114. The clock generator generates two clocking signals each with its own frequency. Thus, if the temperature is too high at the processor chip, the clock generator should change to a lower-frequency clocking signal. (see Col. 6, lines 31-55).

Claim 1, as amended, refers to an external input where an internal clock frequency is reduced if a signal is asserted at the external input. Independent claims 15 and 25 includes similar limitations. Dependent claims (e.g., claims 2, 17, and 26) refer to a situation where the internal clock of the processor is actually stopped (e.g., where the external input is STPCLK input of a Pentium® processor). Neither of these features are shown or suggested by Evoy. Evoy provides a clocking signal input to the processor. A separate chip provides the clocking signal to the processor, where the frequency of that signal is selected based on a perceived temperature. Accordingly an external input that affects the internal clock of the processor as recited in the claims is not shown or suggested by Evoy.

Since features of the claims are missing from and not suggested by the Evoy reference, reconsideration and withdrawal of the rejection of claims 1-30 under 35 U.S.C. §§ 102(a) and 103(a) is respectfully requested.

CONCLUSION

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (202) 220-4200 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,
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Dated: November 29, 2004 By: _____

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